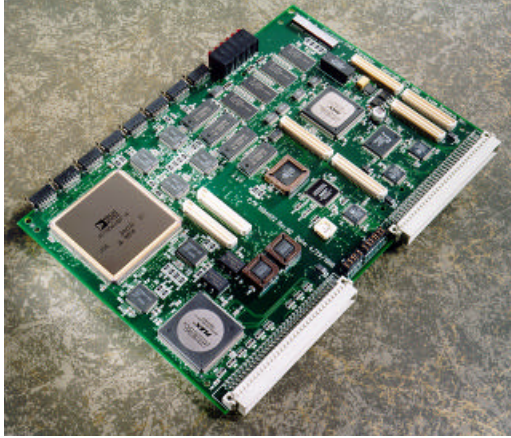


IRVINE SENSORS CORPORATION

Image Processing Systems Group

VIP/Balboa™**Balboa Architecture Image Processor Board****FEATURES:**

- 20 SHARC™ Processors
- Balboa Architecture 320 MB/s, 64 MB
- Single Width, 6U Board
- VME/RACEway™/Link Port I/O
- Direct Video I/O (RS170, RS422)
- IPCE processing to 1 Tear-Op

The **VIP/Balboa** high performance SHARC-based processor board optimizes parallel image and signal processing of large data sets. Combining Analog Devices' AD14060 Quad SHARC MCMs for density and the Balboa Architecture for global access, this 6U VME Processor Board delivers fast parallel processing and flexible system and software integration. It also supports Irvine Sensors' IPCE convolution engines for ultra-fast pattern recognition.

Up to 20 Analog Devices SHARC processors on the VIP/Balboa are connected to a 64 MB global memory and system resources with Irvine Sensors' new Balboa Architecture. Processors can directly access global memory or any system resource on the RACEway backplane. Contention is minimized with the 320 MB/sec Balboa Bus with interfaces to the 64 MB global memory, Video I/O, VME, and RACEway buses. With the Balboa Architecture, system resources are directly and efficiently available to all processors in the SHARC computing fabric.

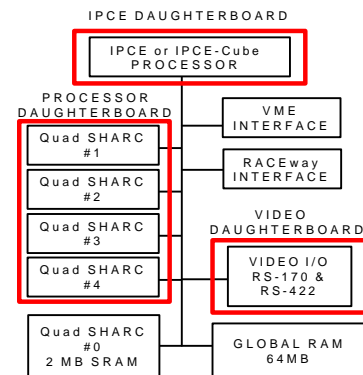
Programming Flexibility:

Direct global access by all processors, and the powerful, multi-processor SHARC computing fabric makes it easy to apply parallel processing to all or parts of large data sets. With the Balboa Architecture, it is no longer necessary to redesign entire algorithms to a data-flow approach to gain parallel processing speed improvements.

IPCE Recognition

VIP/Balboa supports Irvine Sensors' IPCE Convolution Processors that perform up to 10^{12} multiply-accumulate operations per second. With 1,000 times the throughput of the fastest DSP processors, IPCE technology sets a new standard for image and signal recognition systems.

Parallel processing power, fast global access and RACEway compatibility make the VIP/Balboa suited for high speed, image and signal processing for medical, military, and geophysical applications in both new and legacy systems.



For more information, contact National Sales Manager:

Phone: 1-714-549-8211 Fax: 1-714-444-8840 E-mail: vipinfo@irvine-sensors.com

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TECHNICAL SPECIFICATIONS

VIP/Balboa Processor Board	Form Factor	6U VME
	Processor	4 x ADSP-21060, (14060, Quad SHARC MCM), 40 MHz
	SRAM	2 MB SHARC Internal + 512K x 32, zero waitstate
	SDRAM	64 MB, 320 MB/s Global Access
	On-Board Interfaces	Link Ports, Balboa Architecture (Four Balboa Ports)
	Off-Board Interfaces	VME, RACEway, Link Ports (8, Front Panel)
Video I/O Daughterboard (Option V1)	Inputs	4 x RS-170 (NTSC, PAL, SECAM) 10 bit RS422, 16 Bits/pixel, 40 MHz
	Outputs	RS-170 (NTSC, PAL, SECAM) 10 bit RS422, 16 Bits/pixel, 40 MHz
	Throughput	Simultaneous input & output of 1280 x 1024 x 16bits @ 30FPS
	Routing Processor	SHARC ADSP-21062
Processor Daughterboard I (Option 01)	Processors	8 x ADSP-21060 (2 x 14060 Quad SHARC MCM), 40 MHz
	SRAM	4 MB SHARC Internal + 2 x 512K x 32, zero waitstate
	On-Board Interfaces	Link Ports, Balboa Architecture (Two Balboa Ports)
	Off-Board Interfaces	Link Ports (8, Front Panel, 4 to VIP/Balboa Processor Board)
Processor Daughterboard II (Option 02)	Processors	16 x ADSP-21060 (4 x 14060 Quad SHARC MCM), 40 MHz
	SRAM	8 MB SHARC Internal
	On-Board Interfaces	Link Ports, Balboa Architecture (Four Balboa Ports)
	Off-Board Interfaces	Link Ports (8, Front Panel, 4 to VIP/Balboa Processor Board)
IPCE Cube Processor Daughterboard	Processor	Irvine Sensors IPCE3 1,000 GOP (Option 10)
	Image Memory	64 MB, 320 MB/sec access
	Result Buffer	64 MB, 320 MB/sec access
	On-Board Interfaces	Balboa Architecture (One Balboa Port)
	Control Processor	SHARC ADSP-21062

ORDERING INFORMATION

Part Number	Description
VIP-20/B	The VME motherboard is available with a number of SHARC, IPCE and Video I/O configurations. Please contact Irvine Sensors Corporation for availability of specific configurations.

SHARC The Super Harvard Architecture Computer integrates onto a single chip: 120 MFLOP and 40 MIP CPU core (@40MHz), two independent memory buses, 4Mbit (ADSP-21060) on-chip dual ported SRAM, 32-bit FPU, Multiplier and Shifter, scaleable multi-processor support, 240 Mbyte/sec point-to-point communications via six link ports, sophisticated DMA controller and JTAG debugging interface.

Balboa Architecture Irvine Sensor's Balboa Architecture provides FIFO buffered access to the 320 MB/s Balboa Bus for SHARC processors and other system elements. This architecture supports message based transactions between processors, Global RAM, and other system resources. By giving all SHARCs in the compute fabric direct access to global resources, parallel processing solutions can be implemented with minimum restructuring of existing hardware and software systems.

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