

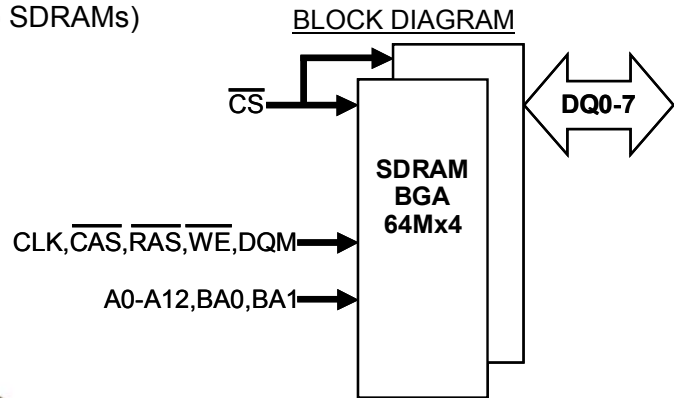
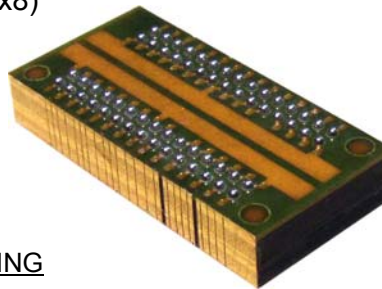
512Mb (64Mbits x 8) SDRAM BGA Memory Stack

GENERAL DESCRIPTION

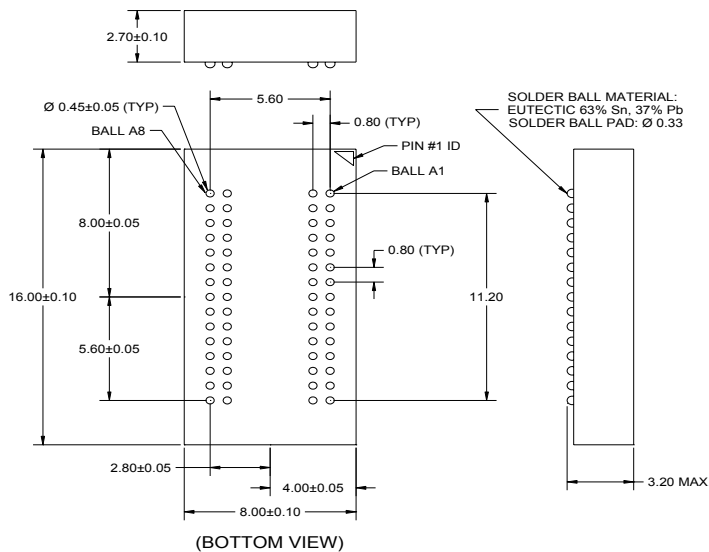
Irvine Sensors Corporation has developed the next generation of stacked memory that fits within the identical JEDEC monolithic outline as a single BGA chip. The 512Mbit Stacked-SDRAM is a high-speed random-access memory. The design of the package allows a simple upgrade path from former products. The features found within a single BGA chip are maintained throughout the Stacked-SDRAM package. Read and write accesses to the Stacked-SDRAM are burst oriented. The Stacked-SDRAM uses an internal pipelined architecture to achieve high-speed operation.

FEATURES

- 512Mbit (Two stacked Micron 256Mbit (32Mbit x 4) SDRAMs)
- Micron Part Number MT48LC64M4A2FB-75
- Identical JEDEC monolithic BGA package outline
- PC-133 compliant
- Fully synchronous
- Self refresh mode
- 64 ms, 8192-cycle refresh
- LVTTTL – compatible inputs and outputs
- Single +3.3V ±0.3V power supply
- Package/Pinout
 - 60-ball FBGA (8mm x 16mm) (x8)
- Timing
 - 7.5ns @ CL=2 (PC133)
 - 7.5ns @ CL=3 (PC133)
- Operating Temperature
 - Commercial (0° C to +70° C)
 - Industrial (-40° C to +85° C)

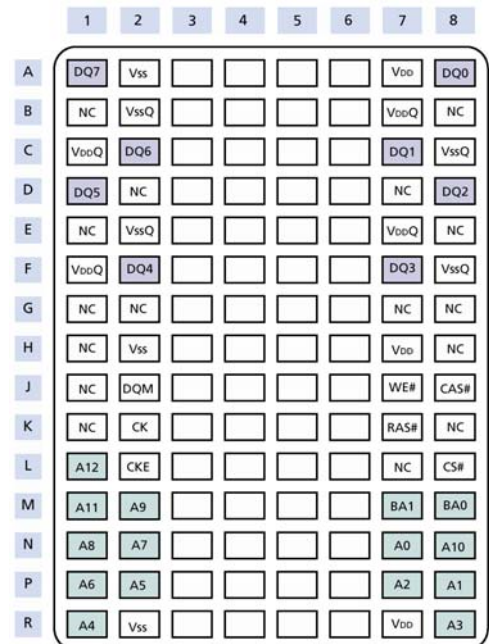


MECHANICAL DRAWING



NOTE: 1. All dimensions in millimeters.
 2. Recommended Pad size for PCB is 0.33mm±0.025mm.

PINOUT DIAGRAM (Top View)



Please refer to Irvine Sensors Web site: <http://www.irvine-sensors.com/BGastack/datasheets> for latest

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*This document contains preliminary information on a product under development. IRVINE SENSORS CORPORATION reserves the right to change product specifications or discontinue this product without prior notice.

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