Neo-Stacking Technology

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Abstract

Irvine Sensors' newest innovation in three-dimensional (3D) packaging is heterogeneous stacks containing all of the components for a complete system or subsystem. The stack is constructed using known good die (KGD), and provides a high level of integration and interconnectivity. This patented packaging technology lends itself to Flash memory and DRAM mass storage, as well as complete computers and other complex embedded systems.

Introduction

Irvine Sensors' established silicon die stacking process starts with complete wafers of chips. A gold reroute metalization is added to bring all signals to an edge, and then the wafer is diced. The dice are stacked, and the stack is lapped in the street area, exposing the ends of the reroute metal. Bus metalization is deposited to the side of the stack, interconnecting the dice and a ceramic top cap substrate, which allows signals into and out of the stack. While this process remains the best solution in many cases, it does have limitations:

Figure 1: Flash Neo-Stack and Layers

- Wafers are sometimes difficult to obtain
- All dice must be the same size, limiting the stack to a single die type
- Dice are not burned in, limiting the stack height or requiring sparing to deal with yields
- Frequent die shrinks require substantial retooling
- The trend in commercial wafers is for street widths to shrink, making the process more difficult

Neo-stacking addresses these limitations and has the following features:

- Starts with known good die (KGD)
- Heterogeneous stack, allowing mixed chip types
- Allows 50 or more thin (10 mil thick) layers
- Accommodates die shrinks easily
- Allows for a high level of interconnectivity
- A largely silicon heat conduction path

Applications for Neo-Stacks are massive memory stacks, "smart" memory modules with built-in logic, drivers, etc., and complete systems in a stack.

Neo-stacking Approach

Start with KGD and bump the die using a gold wire bonder. The wires are pulled off of the gold balls as the bonds are made, assuming that the dice are procured as KGD. For cases when a die type is not available known good, the wires are used for interconnect during test and burn-in, and later removed leaving the ball.

A new wafer, or "Neo-wafer," is constructed using many of the bumped dice in a potting compound matrix. A standard Neo-die size, slightly larger than the largest die in the stack, is used for all dice in the stack. It is this feature that allows the stack to be heterogeneous. Blank silicon is added to open areas on layers where smaller dice are used to enhance thermal conduction between layers. The Neo-wafer is metalized and thinned before dicing into individual Neo-die. Other die types are similarly fabricated into Neo-die of the same dimension. All of the necessary dice are then laminated into a single stack, with all signals to be interconnected brought out to two sides of the stack. On the top of the stack is a substrate, or cap chip, with metalization on both sides, connected through vias. Metalization is added to the two sides of the stack to complete the interconnection between dice, bringing all input/output signals to the cap chip. Figure 1 above shows a 19-Layer Smart Flash Neo-stack and two Neo-layers that are within the stack.

Neo-Wafer Fabrication

Figure 2 shows a cross section of a typical structure for a single large die (e.g., a memory device) in Neo form, with all signals routed to two sides. Figure 3 depicts the same type of Neo-die, from a top view, showing the metalization layout. Figure 5 shows the same die layout in Neo-wafer form before dicing.

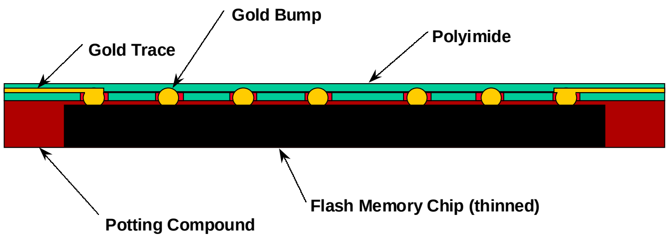

Figure 2: Typical Large Neo-Die Cross Section

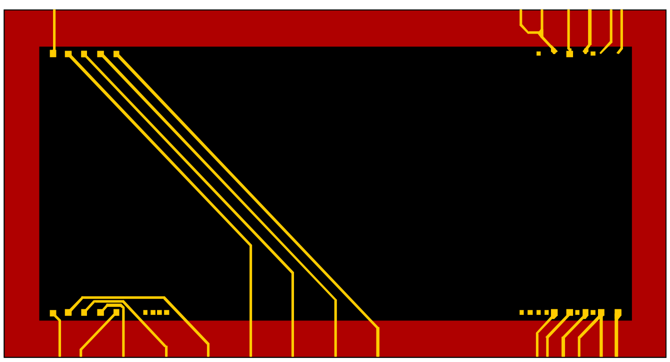

Figure 3: Large Die Neo-die Layout

The Neo-die shown above was fabricated in a Neo-wafer, allowing for a batch processing methodology. The outline dimensions of the Neo-wafer are the same as for standard silicon wafers. This allows standard wafer tooling and fixtures to be used for processes like metalization and thinning.

The new technology allows for multiple dice on a layer, assuming that they are small enough to fit into the standard Neo-die size. A two-layer metalization structure may be necessary to interconnect the dice and exit to the busses. Figures 4 and 5 show the cross section and layout of a typical layer with multiple dice and two-layer interconnection. Note that there are two large pieces of blank silicon in the layer, which help transmit the heat from layers above.

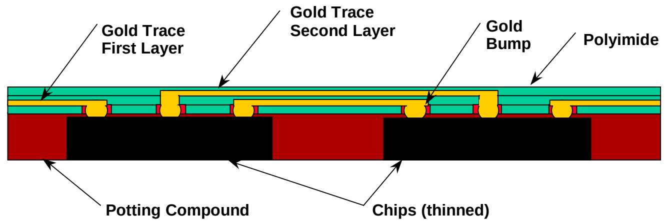

Figure 4: Multi-Dice Layer Cross Section

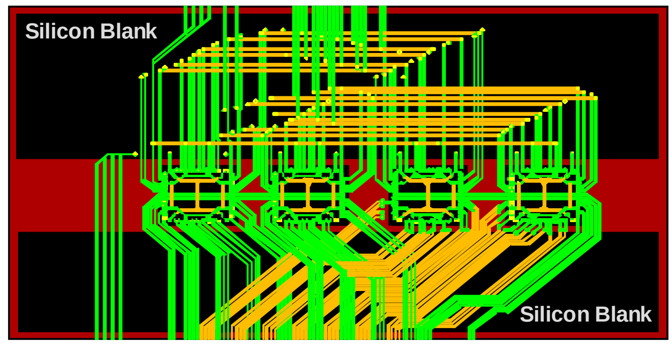

Figure 5: Multi-Dice Layer Layout

Neo-Stacking

Once the Neo-dice are ready, and tested if necessary, they are laminated into a stack. A very thin layer of epoxy between layers holds the stack together. Being very thin (about one micron) allows heat to travel through each adhesive layer without a large temperature change. Figure 6 shows a simple four-layer Neo-stack. Note that the layers are interconnected to each other and to the cap chip using bus metalization on two sides of the stack. Figure 7 shows the Neo-stacking process sequence, starting with Neo-wafers.

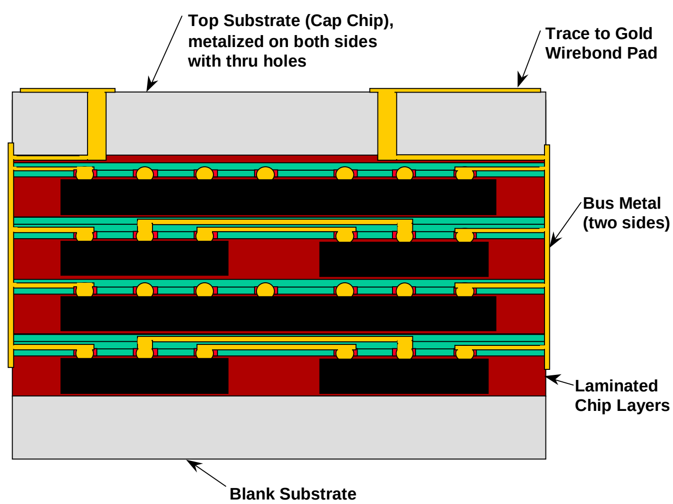

Figure 6: Simple Neo-stack Cross Section

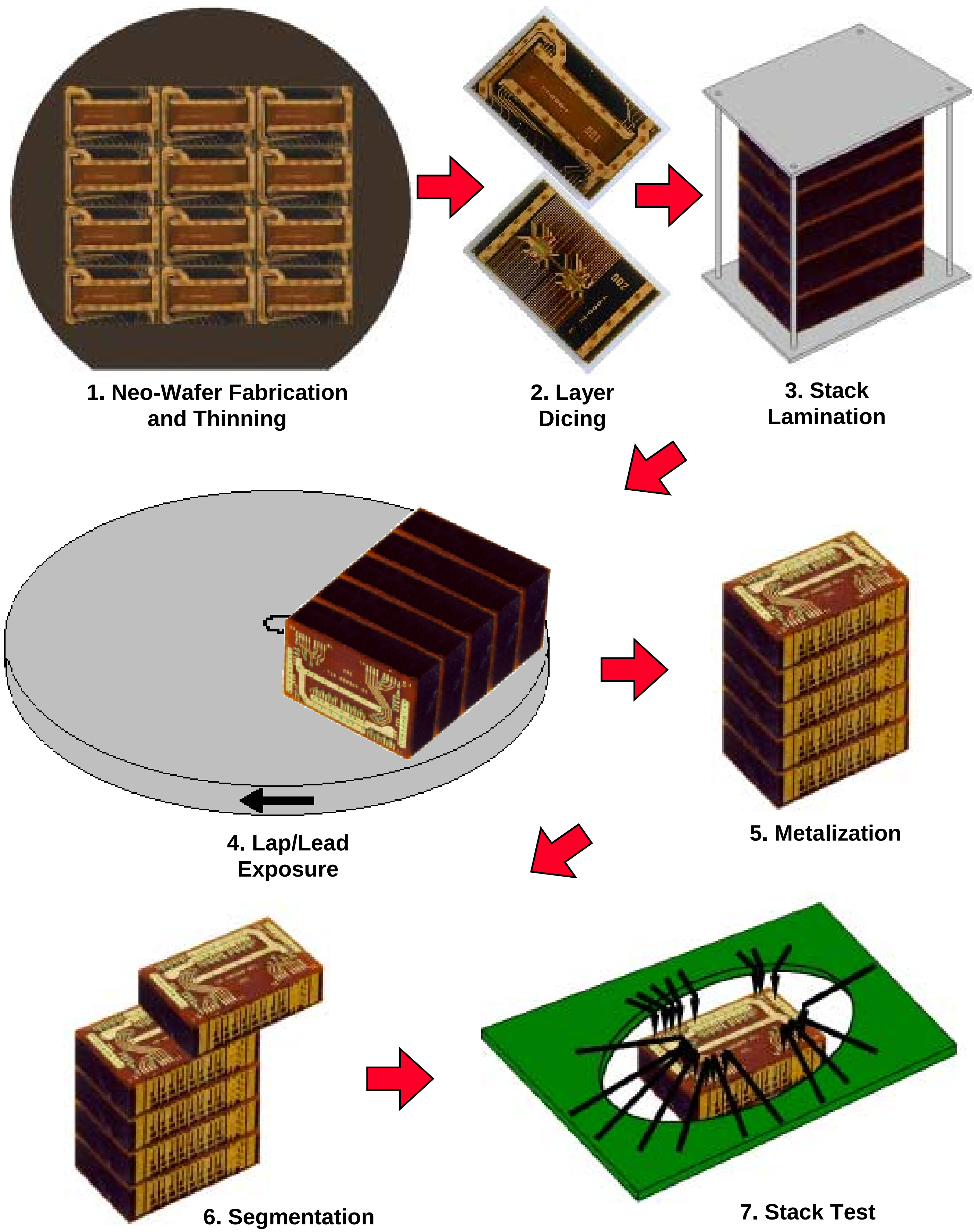

Figure 7: Neo-Stack Process Sequence

Computer-in-a-Stack
Initial development was done under the Advanced Humionics Platform (AHP) Program, which was a DARPA-funded program to develop an advanced wearable computer. Extreme miniaturization was considered necessary for the system to disappear into a soldier's clothing, so as not to hinder movement or interfere with other equipment.

Irvine Sensors designed the computer stacks, confirming the feasibility and potential of the technology. A single stack is a complete computer with 52 chips on 48 layers, and includes 10 chip types. This includes a processor, interface chips, DRAM, and 32 layers of Flash memory for mass storage, eliminating the need for a hard drive. All of this is in an envelope that measures 0.8" x 0.5" x 0.5" high. Also included in the stack are precision resistors and capacitors, fabricated on silicon and processed in the stack in the same way as a chip. This design demonstrates that complex embedded systems requiring a high level of interconnectivity can be designed as Neo-Stacks.

Demonstration Vehicles
A significant portion of the design described is being built. It includes 16 layers of Flash memory and the associated control and drive circuitry. The Flash module is shown in Figure 8.

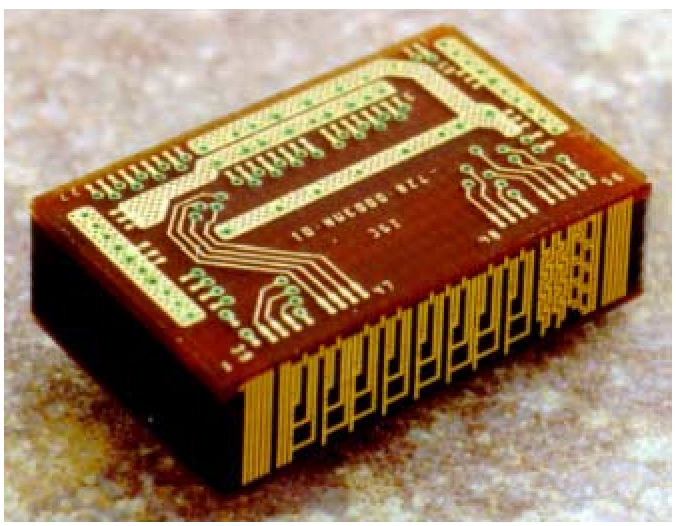

Figure 8: Flash Memory Module

Neo-stacking is not confined to standard silicon chip types. A system including lasers and detectors for optoelectronic switches has been demonstrated at the layer level. This layer is shown in Figure 9.

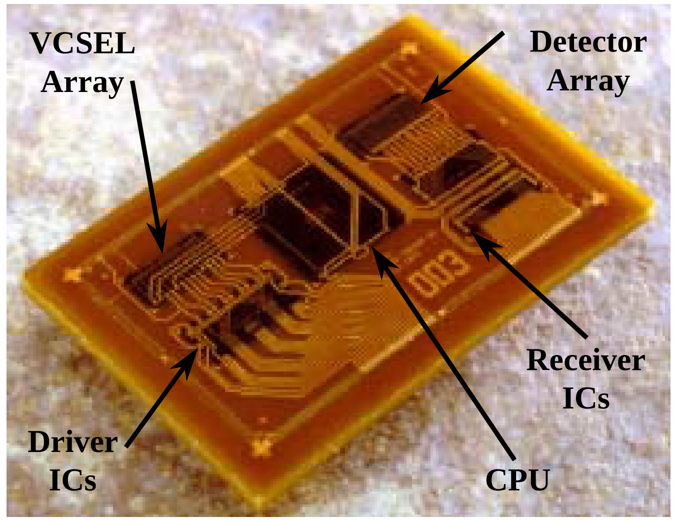

Figure 9: Embedded Optoelectronic System

Summary
Neo-stacking is a breakthrough in high density packaging technology. It allows different size, technology, and function ICs to be stacked and integrated in an extremely miniaturized unit. The resulting stack is an ultra-high-density, complete embeddable system with a high level of interconnectivity. It is the consummate 3D packaging technology. □

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Irvine Sensors Corporation (NASDAQ: IRSN and the Boston Stock Exchange: ISC) is the inventor of three-dimensional (3D) semiconductors and the SIRComm™ technology used for wireless infrared (IR) communications, the Silicon MicroRing Gyro™ for MEMS motion sensing, and the Electronic Film System™ (EFS™) image capture system. Founded in 1980, the company pioneered the development of advanced signal processing and image stabilization technologies for focal planes. Today, Irvine Sensors continues to develop advanced technologies for 3D stacked integrated circuits (ICs), IR and general signal processing, smart sensors, image processing and recognition, low-power analog and mixed signal ICs, miniature cameras, high density interconnections, photonics communications, and image stabilization for electronic systems. The company holds over 50 U.S. and foreign patents.

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