IRVINE SENSORS CORPORATION

SILICON BRAIN ARCHITECTURE

Special Technical Summary: 3D Field-Effect Transistor (3DFET)

An electronic assembly that emulates the human functionality of recognition and simple decision making is needed almost in all future applications. Researchers and developers around the world are working on pieces of this problem. The silicon neuromorpic sensors at Cal Tech, neural circuits at JPL, photonic interconnectivity at UCSD and USC, and the algorithmic architectures at Boston University are important examples. The 3D silicon stacking technology is important to provide the very short distance, completely parallel interconnectivity that enables the silicon brain to achieve peta-ops performance for under 10 watts. The generic silicon brain architecture is shown in Figure 1. Thinned and stacked integrated circuit chips emulate the highly integrated neural circuitry of the brain. These circuits are weighted synapse arrays (WSAs) terminating in neurons connected to other WSAs. Crossbar switches in each chip enable all possible interconnects within and between stacks. The outer peripheral stacks interface with sensor chips - imaging optical "retinas", auditory "cochlea's", and digital or analog buses connected to arbitrary sensors nearby or remote. A bus and control plane analogous to the brain mid-line plane separates the two halves of the silicon brain and provides clock signals, ground, power and inter-lobe communications.

The list of the technologies involved and the roadmap towards the silicon brain is shown in Figure 2. Among the technologies listed some of the most important ones contributed directly by Irvine Sensors are cascaded neural processing modules, new spatial and temporal WSAs with embedded crossbar switches, and 3DFET interconnects. The 3DFET interconnect is a conceptual breakthrough to resolve layer-to-layer high density I/O problem with ramifications that extends beyond the silicon brain program. Therefore, Silicon Brain Architecture SBIR Phase II efforts will be concentrated in demonstrating the 3DFET concept in conjunction with other inter-related high-density integration technologies to achieve the silicon brain.

Based on a related development at CalTech to emulate visual cortex using FPGAs (field programmable gate arrays), a stacked FPGA approach was selected for the Silicon Brain Architecture SBIR Phase II silicon brain emulation. The use of FPGAs is important because many potential custom IC configurations can be implemented without committing funds to expensive IC design and development. The difficulty with the conventional FPGA-based implementations of large electronic functionality is that advanced FPGAs have several hundreds pin-outs each and to obtain enough gate count in a stack will require several chips to be interconnected resulting in over several thousands of interconnects. The 3DFET concept fits

Irvine Sensors Corporation, 3001 Redhill Avenue, Building 3; Costa Mesa, CA 92626-4529
Website: www.irvine-sensors.com Phone: 1-714-549-8211
E-mail: lomara@irvine-sensors.com Fax: 1-714-557-1260

nicely with stacked FPGAs by allowing dense interconnects between the layers. A new implementation of 3DFET, named hybrid 3DFET is considered for Silicon Brain Architecture SBIR Phase II. The hybrid 3DFET uses a ceramic feed-through chip for the gate side and a tiny silicon chip as the source and drain side of the 3DFET. The combination of hybrid 3DFET with FPGAs and field programmable interconnect devices (FPIDs) using ISC's newly developed neo-chip technology, will allow us to realize core processing functions in a very flexible Silicon Brain Architecture SBIR Phase II demonstration vehicle. The insertion of the FPIDs will allow the stack interconnections to be totally reconfigurable. Therefore, different interconnect schemes such as mesh, butterfly, crossbar can be implemented on-request and on-the-fly between the processing nodes formed in FPGAs without any hardware changes. This flexibility of the resulting stack can be used to rapidly prototype any digital processor. Such a powerful module with on-the-fly change of processing functionality has large commercial viability.

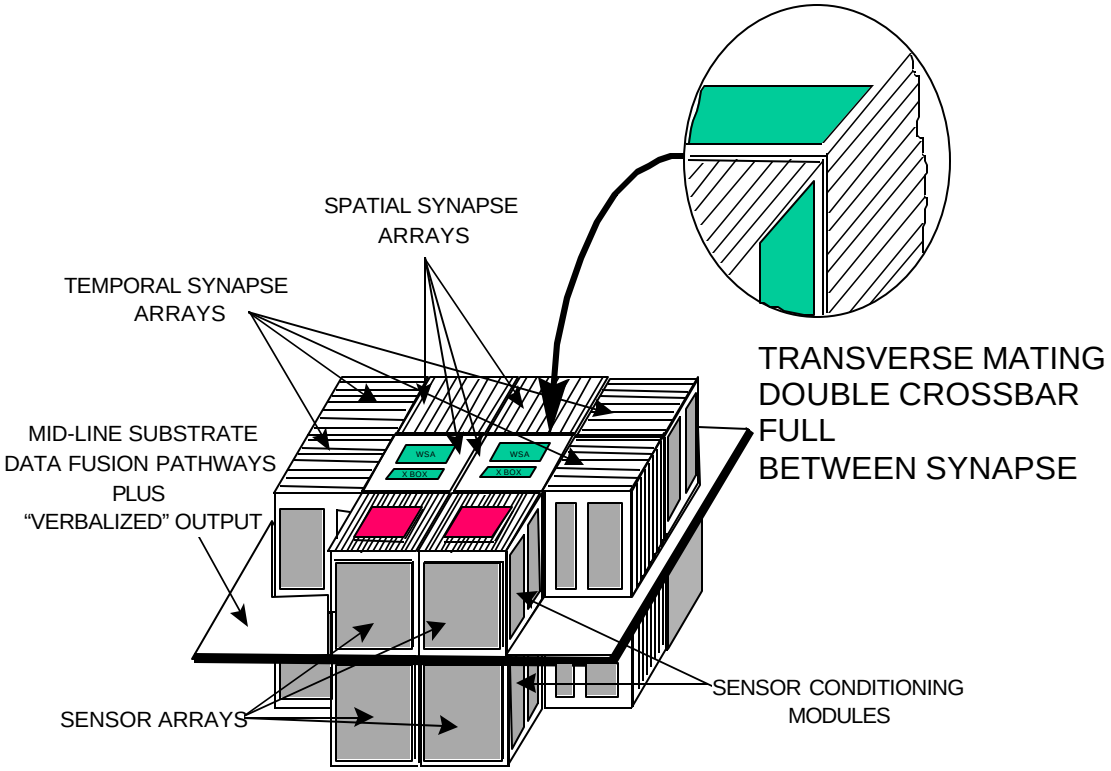

Figure 1. The general concept of Silicon Brain: a prototype with a total of 512 stacked layers is expected to deliver 80 petaflops at 20 W.

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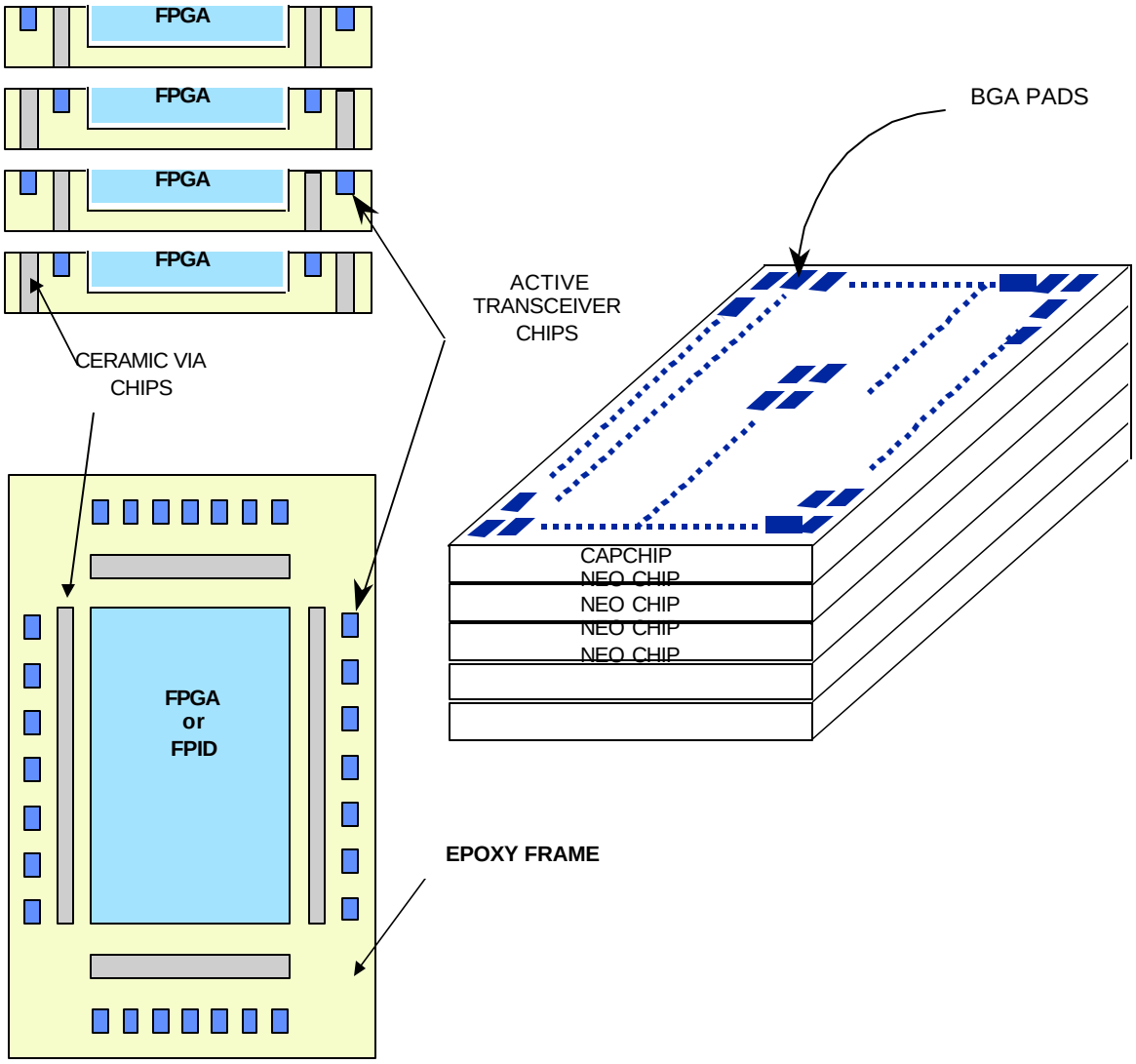

Figure 2. The demonstration article to be used for the Silicon Brain Architecture SBIR Phase II will consist of FPGAs, FPIDs and active tranceiver chips using the hybrid 3DFET concept. Besides validating all of the Silicon Brain related concepts, this module has commercial viability due to its ability to emulate digital processors.

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